

Silicon NPN Power Transistors

2SC1108

DESCRIPTION

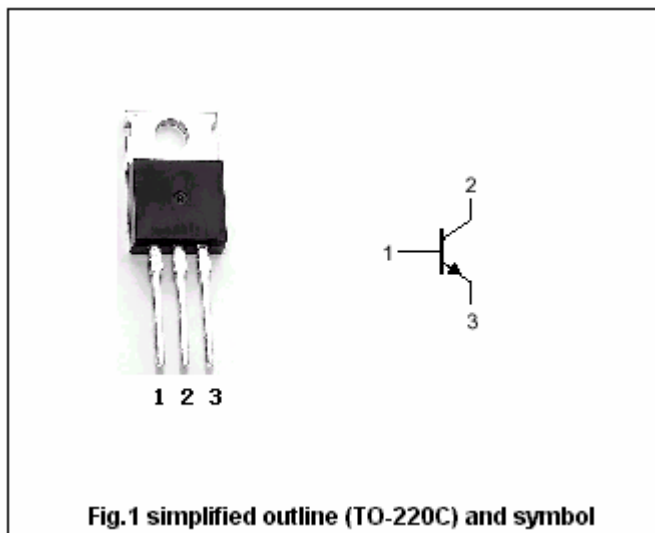
- With TO-220C package
- High breakdown voltage : $V_{CE0}=100V$
- High current :4A

APPLICATIONS

- For power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

**Absolute maximum ratings($T_c=25^\circ$)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	100	V
V_{CEO}	Collector-emitter voltage	Open base	100	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		4	A
P_C	Collector power dissipation	$T_C=25^\circ$	40	W
T_j	Junction temperature		150	?
T_{stg}	Storage temperature		-55~150	?

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CHARACTERISTICS

T_j=25? unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =25mA; I _B =0	100			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =3A; I _B =0.3 A			1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =3A; I _B =0.3 A			2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =100V; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =4V	100		320	
f _T	Transition frequency	I _C =0.5A ; V _{CE} =12V		10		MHz
C _{OB}	Output capacitance	I _E =0; V _{CB} =10V; f=1MHz	25			pF

PACKAGE OUTLINE

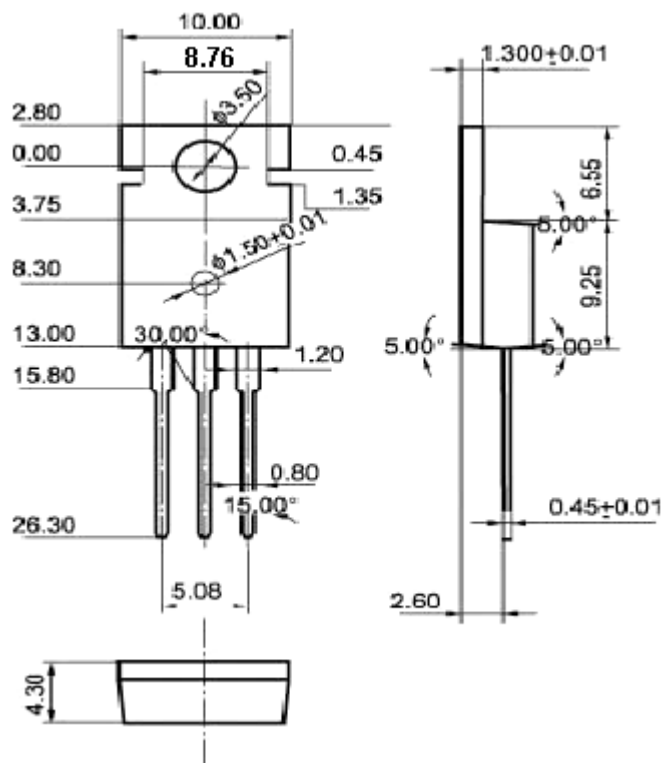


Fig.2 Outline dimensions (unindicated tolerance:±0.10 mm)